

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Constantin Bulucea
Assignee: National Semiconductor Corporation
Title: Gate-Enhanced Junction Varactor
Serial No.: 09/903,059 Filing Date: July 10, 2001
Examiner: D. Farhani Group Art Unit: 2814
Docket No.: NS-4971 US

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San Jose, California
19 December 2002

COMMISSIONER FOR PATENTS
Washington, D. C. 20231

AMENDMENT

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Sir:

Responsive to the Office Action mailed 28 August 2002, please amend the above patent application as follows. A one-month extension of time accompanies this Response, allowing the Applicants until 28 December 2002 to respond.

IN THE CLAIMS

Amend Claims 20, 23, 29, 31, 32, 38, 43, 44, and 50 to read:

--20. (Amended) A structure as in Claim 19 wherein the plate region occupies a lateral plate area along the primary surface, the varactor has a minimum capacitance dependent on the plate area, an inversion layer that meets the plate region selectively appears and disappears in the body region below the gate electrode, do as to the left and right of the plate area.

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